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WHAT IS CLAIMED IS:

1. A semiconductor memory device comprises:

a memory array having plurality of word-lines arranged in a predetermined direction and in parallel to each other, a plurality of bit lines arranged orthogonally to a plurality of the word-lines and in parallel to each other, and a plurality of memory cells arranged at predetermined intersection points of a plurality of the word-lines and a plurality of the bit-lines, the number of the predetermined intersection points being equal to half of all the intersection points;

a plurality of switches connected to one-side end of the bit-lines provided at an odd-numbered position of a plurality of the bit-lines and connected to the other-side end of the bit-line provided at an even-numbered position, respectively; and

a plurality of unit circuits each having two terminals connected to a pair of odd-numbered or even-numbered bit lines of a plurality of the bit lines, the unit circuits being arranged in a column in a predetermined direction in the vicinities to the both ends of a plurality of the bit lines, respectively,

the predetermined intersection points being determined in such a manner that when one of a plurality of the word lines is selected, the memory cells of a plurality of the memory cells connected to the selected word line can be electrically connected, one by one, to the terminals of a plurality of the unit circuit.

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2. A semiconductor memory device according to Claim 1, wherein when one of a plurality of the word lines is selected, the switches operates so that the memory cells connected to the selected word line are electrically connected to the terminals of the unit circuits, respectively.

3. A semiconductor memory device according to Claim 1, wherein a plurality of the switches are MOS transistor switches in which two switches are integrated with each other, respectively.

4. A semiconductor memory device according to Claim 3, wherein each MOS transistor switch contains two gate electrodes arranged in parallel to each other, two drain regions formed on both sides of the gate electrodes, independently from each other, and a single source region formed between the two gate electrodes, a pair of the odd-numbered or even-numbered bit lines are connected to the two drain regions, respectively, and a terminal of each unit circuit is connected to the source region.

5. A semiconductor memory device according to Claim 1, wherein each memory cell comprises one cell-use MOS transistor and one capacitor.

6. A semiconductor memory device according to Claim 5, wherein the cell-use MOS transistor is formed on a substrate doped into a p-type, and contains as a gate electrode a polySi layer doped with a p-type impurity.

7. A semiconductor memory device according to Claim 6, wherein each unit circuit contains a first MOS transistor which is formed on a substrate doped into a p-type and has

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a first polySi layer doped with a n-type impurity, and a second MOS transistor which is formed on a substrate doped into a n-type and has as a gate electrode a second polySi layer doped with a p-type impurity.

8. A semiconductor memory device according to Claim 6, further comprising a peripheral circuit for controlling the cell array and a plurality of the switches, the peripheral circuit containing a first MOS transistor which is formed on a substrate doped into a p-type, and has as a gate electrode a first polySi layer doped with an n-type impurity, and a second MOS transistor which is formed on a substrate doped into an n-type, and has as a gate electrode a second polySi layer doped with an p-type impurity.

9. A semiconductor memory device according to Claim 5, wherein each word line comprises a first wiring layer using for the gate electrode of the cell-use MOS transistor and a second wiring layer having a lower resistance than the first wiring layer and backing the first wiring layer at predetermined positions.

10. A semiconductor memory device according to Claim 5, wherein each word line comprises a first wiring layer using for the gate electrode of the cell-use MOS transistor, a drive circuit for driving the first wiring layer, and a second wiring layer connected to the drive circuit and having a lower resistance than the first wiring layer.

11. A semiconductor memory device according to Claim 1, wherein the unit circuits are connected, in addition to the above-described memory cell array, to another memory cell array having the same constitution as the above-

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described memory cell array.

12. A method of testing the semiconductor memory device defined in Claim 1 comprising the step of: selecting a plurality of the word lines sequentially one by one, and turning-on all of a plurality of the switches.

13. A method of testing the semiconductor memory device defined in Claim 1 comprising the steps of; selecting a plurality of the word lines sequentially one by one, and controlling a plurality of the switches so that the memory cell is electrically connected to only one terminal of each of a plurality of the unit circuits: and thereafter, again, selecting a plurality of the word lines sequentially one by one, and controlling a plurality of the switches so that the memory cell is electrically connected to only the other terminal of each of a plurality of the unit circuits.